Description

Delay locked loop and a method for delay control

The present invention relates in general to a method and an apparatus for the provision of clock signals in circuit units, and relates in particular to a method and an apparatus for delay control of clock signals within circuit units, which are related in time to an external clock signal.

The increasing packing densities and physical sizes of integrated circuits are creating a need to provide a clock signal distribution and a clock signal delay extremely precisely on the chip - "on-chip". Phase locked loops (PLLs) and delay locked loops (DLLs) are used for adjustable timing with respect to the clock signals that are used.

Conventionally, delay locked loops (DLLs) such as those described in the publication www.xilinx.com dated 5 July 2002, are preferred for delay compensation and clock conditioning. Phase locked loops provide a propagation delay from zero for a very small clock shift between output clock signals which have to be distributed in a circuit unit.

A conventional delay locked loop for an SDRAM using digital components is described, for example, in the publication "IEEE, Journal of Solid-State Circuits, Vol. 32, pages 1728-1997, November 1997".

Delay locked loops and phase locked loops based on self-biased techniques are described in the publication "IEEE, Journal of Solid-State Circuits, Vol. 31, pages 1723-1732, November 1996".

One major disadvantage of known delay locked loops is that the delay locked loop is essentially a delay line which has to internally interpolate the external clock, which means that it must be able to match itself to input signals at all the possible frequencies. This means a time delay in a delay line must be longer than one clock cycle at the lowest frequency.

A further disadvantageous feature is that high resolution is required towards the higher frequencies, in order to achieve good data matching. The use of the same delay locked loop to cover low and high frequencies means that the delay line has to include a very large number of delay elements. If, by way of example, a delay time resolution of 20 pikoseconds (ps) is required, and the delay line is required to have an overall delay of 20 nanoseconds, then a total of N = 20 ns/25 ps = 800 individual elements are required in series. Such a large number of delay elements results in further problems, such as large circuit designs and excessive power consumption. Further problems then result with the signal timing and the circuit design for a structure with a large number of elements.

One object of the present invention is therefore to provide a delay locked loop which can be used equally well for low and high frequencies and which has a simple circuit design.

According to the invention, this object is achieved by a delay control apparatus having the features of Patent Claim 1. The object is also achieved by a method as specified in Patent Claim 8.

Further refinements of the invention can be found in the dependent claims. One major idea of the invention is to obtain prior knowledge of the frequency range in which an input signal that is to be delayed is located.

Knowledge such as this allows a delay time to be set approximately, while the fine adjustment can conventionally be carried out by means of a delay locked loop.

The essence of the invention is to provide an additional frequency detection unit which acts on a delay time of a second delay element, which is connected in series with the conventional delay element. This allows flexible delay time control to be achieved equally well for low and high frequencies, with a simple circuit design.

The delay control apparatus according to the invention for provision of clock signals in circuit units, in which the clock signals within the circuit units can be predetermined variably in time with respect to an external clock signal, essentially has:

a) a delay device comprising a first delay element for provision of a variable time delay between an output signal and an input signal for the first delay element;

b) a feedback device to which the output signal is supplied, for feeding back the output signal, in which the feedback device emits a time-delayed, fed-back output signal; and

c) a phase difference detection device, for detection of a phase difference between the input signal and the fed-back output signal, in which the phase difference detection device emits a control signal for controlling the delay element as a function of the detected phase difference, in which the delay control apparatus also has at least one second delay element which is connected in series with the first delay element, and a frequency detection unit for detection of the frequency of the input signal, in which the second delay element

can be adjusted as a function of the detected frequency of the input signal.

Advantageous developments and improvements of the respective subject matter of the invention can be found in the dependent claims. According to one preferred development of the invention, the delay control apparatus has a filtering device for filtering the control signal which is emitted from the phase difference detection device.

According to yet another preferred development of the present invention, the feedback device has a time delay which corresponds to the sum of a receiver time delay that is caused in the receiver and a driver time delay that is caused in the driver (OCD, Off Chip Driver), that is to say sum = Trcv + Tocd.

According to yet another preferred development of the present invention, a second delay element for low frequencies of the input signal, and at least one further second delay element for high frequencies of the input signal, are provided in the delay device. The same delay device can advantageously be used for high and low frequencies, just be switching over the second delay element.

According to yet another preferred development of the present invention, the delay device is formed by at least one capacitor element which is varied by means of a control voltage.

According to yet another preferred development of the present invention, the delay device is formed by at least one current inverter which is varied by means of a control voltage. According to yet another preferred development, the delay device is formed by an inverter chain.

Furthermore, the method according to the invention for provision of clock signals in circuit units in which the clock signals within the circuit units are predetermined variably in time with respect to an external clock signal, has the following steps:

a) provision of a variable time delay between an output signal and an input signal of a delay device with a first delay element;

b) feedback of the output signal by means of a feedback device to which the output signal is supplied, in which the feedback device emits a time-delayed, fed-back output signal, and

c) detection of a phase difference between the input signal and the fed-back output signal by means of a phase difference detection device to which the input signal and the fed-back output signal are supplied, in which the phase difference detection device emits a control signal for controlling the first delay element as a function of the detected phase difference, in which the frequency of the input signal is detected by means of a frequency detection unit, and in which at least one second delay element, which is connected in series with the first delay element, is adjusted as a function of the detected frequency of the input signal.

According to yet another preferred development of the present invention, in order to allow the frequency detection unit to adjust the time delay of the second delay element, the cycle time of the delay control apparatus is compared with a number, which can be predetermined, of delay units for the second delay element. The number of delay units for the second delay element is expediently eight.

According to yet another preferred development of the present invention, the delay control apparatus is reset by means of a reset pulse before frequency detection by means of the frequency detection unit.

According to yet another preferred development of the present invention, an overlap area is provided between adjacent detection frequency ranges.

According to yet another preferred development of the present invention, the output signal is delayed by the sum of a receiver time delay and of a driver time delay for feeding back in the feedback device, to which the output signal is supplied.

According to yet another preferred development of the present invention, the control signal which is emitted from the phase difference detection device is filtered in a filtering device for the delay control apparatus.

Exemplary embodiments of the invention will be explained in more detail in the following description and are illustrated in the drawings, in which:

Figure 1 shows an illustration of the reading/writing of data in a dynamic random access memory (DRAM) at twice the data rate (DDR, Double Data Rate);

Figure 2 shows a delay control apparatus with a frequency detection unit according to one preferred exemplary embodiment of the present invention;

Figure 3 shows a schematic illustration of the delay times which occur in the delay control apparatus, which is in the form of a delay locked loop;

Figure 4 shows the timing diagram for a delay time control with upstream frequency detection;

Figure 5 shows an overlap area between a low detection frequency range and a high detection frequency range in the delay control apparatus;

Figure 6(a) shows an example of a variable delay device based on a variable, voltage-dependent capacitor;

Figure 6(b) shows an example of a delay device based on a current inverter which is varied by means of a control voltage;

Figure 6(c) shows an example of a delay device based on an inverter chain;

Figure 7(a) shows an illustrative example of a frequency detection unit;

Figure 7(b) shows a timing diagram of the clock signals which occur in the circuit diagram shown in Figure 7(a);

Figure 8 shows a further example of a circuit arrangement for frequency detection;

Figure 9(a) shows a flowchart for low input signal frequencies for the circuit arrangement shown in Figure 7; and

Figure 9(b) shows a flowchart for high input signal frequencies for the circuit arrangement shown in Figure 7.

Identical reference symbols denote identical or functionally identical components or steps in the figures.

Figure 1 shows the purpose of the method according to the invention and of the apparatus according to the invention on the basis of a delay locked loop for provision of clock data in a DRAM which is written to and read from at twice the data rate (DDR). Different clock flanks are predetermined as a function of a clock signal 220. In the DDR method, even-numbered DDR data 218 is addressed by means of an even-numbered DDR clock flank 216, while odd-numbered DDR data 219 is addressed by means of an odd-numbered clock flank 217. As can clearly be seen, these clock flanks must be positioned very precisely with respect to the data stream, and must not be in the form of an asynchronous data stream 221 as shown, by way of example, on the left in Figure 1.

In order to provide flexible clock signal production for a DRAM memory and in order in particular to make it possible to operate in a wide frequency range from 50 MHz (20 ns) up to 500 MHz (2 ns), exact delay timing is required by means of a suitable delay control apparatus.

Figure 2 shows a delay control apparatus according to one preferred exemplary embodiment of the present invention. This illustration shows an input signal 103 being input into the delay control apparatus and being received by a data stream receiver (RCV) which is not shown. After the processing in the delay control apparatus, the clock signal is provided as an output signal 104 from an external driver device (OCD, Off-Chip Driver, not shown), which is not arranged on the chip. The time delay for the input signal 103 is

provided by means of a delay device 100, with the delay device 100 having a first delay element 101 and a second delay element 102.

The first delay element 101 is in the form of a variable delay element, whose delay time can be varied by means of a control signal 109 or a filtered control signal 109'. The delay time of the second delay element 102 can be adjusted in discrete steps, and produces an approximate time delay. The design of the delay locked loop and of the delay control apparatus will be described briefly in the following text. The output signal 104 is fed back via a feedback device 106. In the feedback device 106, the output signal 104 has applied to it, for example, a time delay which corresponds to the sum of a receiver time delay 201 and of a driver time delay 203, as will be explained in the following text with reference to Figure 3.

A time-delayed, fed-back output signal 107 which is emitted from the feedback device 106 is supplied in the same way as the original input signal 103 to a phase difference detection device 108. The phase difference detection device 108 is used to detect the phase difference between the input signal 103 and the fed-back output signal 107, and to emit a control signal 109 which is dependent on the phase difference.

As is illustrated in the exemplary embodiment shown in Figure 2, the control signal 109 is supplied to a filtering device 111, which emits the filtered control signal 109'. The filtered control signal 109' varies the first delay element 101 until the phase difference between the input signal 103 and the fed-back output signal 107 is cancelled out. The overall delay time is governed by the delay time of the first delay element 101 and the delay time of the second delay element 102. The second delay element 102 is adjusted by means of an

output signal from a frequency detection unit 110, that is to say a second delay time is set in the second delay element 102 as a function of the frequency of the input signal 103 as detected in the frequency detection unit 110. According to the invention, it is now expedient to provide different second delay elements 102 and different delay times for the second delay element 102 for different frequency ranges, as described in the following text with reference to Figure 5.

As described in the following text with reference to Figure 3, the overall delay time of the delay control apparatus is a function of the frequency of the input signal 103, so that in the event of a frequency change or in the event of a change to the frequency of the input signal 103, the overall delay time must be changed.

Figure 3 shows, schematically, the composition of the overall delay time 204. The overall delay time is the sum of a receiver time delay 201, which occurs in the data stream receiver and is caused by the variable time delay 105 produced by the delay control device and a path time delay 202 which is caused by a data FIFO path, and a driver time delay 203 which is caused by the time delay to/in the Off-Chip-Driver. The overall time delay is thus given by the following formula:

$$T_{201} + T_{105} + T_{202} + T_{203} = N \cdot T_{cycle(f)}.$$

The cycle time T_{cycle} is governed by the external clock, and a function of the frequency of the input signal 103; N is an integer, that is to say the cycle time T_{cycle} must correspond to a multiple of the overall time delay 204.

In accordance with the method according to the invention, frequency detection is now carried out by means of a frequency detection unit 110, before the operation of the delay locked loop starts.

In this case, it is not important to know the exact value of the frequency of the input signal 103 (see Figure 2), but only the order of magnitude of the frequency of the input signal 103. There may be two or more of the second delay elements 102 as shown in Figure 2, for example for a low frequency (long delay) and for a high frequency (short delay), in order to use the delay locked loop for a broad frequency range.

As is illustrated in Figure 4, the frequency of the input signal 103 is checked before the start of operation of the delay locked loop. For this purpose, the delay control apparatus is first of all reset by means of a reset pulse 209, in order to provide a frequency detection start 206. For example, eight delay units 205 correspond to eight clock cycles of the detected input signal. The delay control mode 208 starts at the end 207 of frequency detection. After each reset pulse 209, a new frequency detection process is carried out by means of the frequency detection unit 110.

As mentioned above, two different second delay elements 102 may, for example, be provided, in order to cover a low frequency range and a high frequency range, as is illustrated schematically in Figure 5. Two different frequency detection ranges 211, 212 overlap in an overlap area 210, which occurs at an intermediate frequency 214. The first detection frequency range 211 thus occurs between a low frequency 213 and the intermediate frequency 214, while the second detection frequency range 212 occurs between the intermediate frequency 214 and the high frequency 215. The two

frequency ranges are covered by two different second delay elements 102.

Figures 6(a) to 6(c) show different circuit arrangements for provision of a variable time delay. Figure 6(a) shows a delay device 100, which is formed by two capacitor elements 305 which are driven by means of a control voltage 304. The capacitor elements are each connected between the junction points of individual inverter elements 301 and 302 and ground, with the inverter elements 301, 302 etc. forming an inverter chain. The application of the control voltage 304 results in the capacitor elements 305 having a variable capacitance and, in conjunction with the inverter chain comprising the inverter 301, 302 etc., providing a time delay for the output signal 104 with respect to the input signal 103.

Figure 6(b) shows, schematically, a circuit arrangement for a current inverter, which is varied by means of a control voltage 304. The effect of the circuit arrangement shown in Figure 6(b) is similar to that of the circuit arrangement shown in Figure 6(a), with the output signal 104 being delayed in time with respect to the input signal 103 as a function of the control voltage 304. Figure 6(c) shows a further variant of a time delay, which can be predetermined such that it is fixed, by means of an inverter chain, with different and differently delayed output signals 104 and 104a being obtained from an input signal 103 by combining inverter elements 301, 302 and 303.

Figures 7(a) and 7(b) show a circuit arrangement and a flowchart, which are required for frequency detection. A clock input signal 403 and an inverted clock input 404 are respectively supplied directly and via an inverter chain 401 or 402 to the two respective inputs of a NAND gate 409 or 410. The outputs of the two NAND

gates are supplied to the two NAND gates 407 and 408 of a locking gate 413, which produces a clock output signal 405 and an inverted clock output signal 406. The operation of the circuit arrangement shown in Figure 7(a) will be explained with reference to Figure 7(b). The locking gate changes its logic state whenever positive flanks occur on the one hand in the clock input signal 403 and on the other hand in the inverted clock input signal 404. This results in a regular clock output signal 405 and a regular inverted clock output signal 406, with half the period duration corresponding to a flank difference time between the two clock input signals 403 and 404. A good estimate of the cycle time (T_{cycle}) is obtained in accordance with the following formula from a measurement of the flank difference time 417 (T_{417}):

$$T_{cycle} \approx 2 \cdot T_{417}.$$

On the basis of the above formula, the cycle time and hence the frequency of the input signal which is applied to the delay control apparatus are known. This can be used, as explained above with reference to Figure 2, to adjust the second delay element 102.

Figure 8 shows a further method for determination of the frequency of the input signal 103 in the frequency detection unit 110, in order to carry out the method according to the invention for adjustment of the delay control apparatus. A clock input signal 403 is supplied to a reference delay device 412 and, as a gate signal 416 is supplied to a locking gate 413. An inverted clock input signal 404 is supplied directly to a clock generator 411.

The clock generator is also supplied with the clock input signal 403, delayed in the reference delay device 412, as a delayed clock input signal 414. It should be

mentioned that the reference delay device is formed from individual reference delay elements 412a, 412b, 412c and 412d, for example four such elements. This results in a similar way to the method described with reference to Figures 7(a), (b) in a clock generator output signal 415 which is supplied to the locking gate 413. The output signal from the locking gate 413 once again provides information about the flank difference time 417.

The following text considers two operating states in order to determine the flank difference time 417, as are shown in Figure 9(a) for low frequencies and in Figure 9(b) for high frequencies. For the low frequency (Figure 9(a)), the delay between the rising flank of the clock input signal 403 and the rising flank of the inverted clock input signal 404 is greater than the fixed delay, as can be seen from the delayed clock input signal 414. The event (i) therefore occurs, that is to say the flank of the delayed clock input signal 414 rises before the event (ii), that is the say the rise in the clock flank of the inverted clock input signal 404.

This means that the clock spends longer than the fixed delay time at a high level and, in consequence, the clock period is two or more times the fixed delay.

At the high frequency (Figure 9(b)), the event (i) occurs after the event (ii), so that the period is shorter than twice the fixed delay. This results in a clock generator output signal 415 in Figure 8 being a signal which spends a long time period at a 1-level, as is desirable for low frequencies (Figure 9(a)) while, as is shown in Figure 9(b), the clock generator output signal 415 for high frequencies is a short pulse.

This means that the delay control apparatus sets a long time delay in its second delay element 102, for detection of low frequencies, while the delay control apparatus sets a short time delay in its second delay element 102 for high frequencies. This allows the delay locked loops to be matched in an advantageous manner to the broad frequency range of the input signal.

Although the present invention has been described above on the basis of preferred exemplary embodiments, it is not restricted to them but can be modified in many ways.

The invention is also not restricted to the cited application options.